IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A method of cooling a semiconductor chip, comprising:

providing a number of electrical devices on a semiconductor layer of a flip-chip configuration semiconductor chip;

integrally forming a substantially planar heat conducting layer on only a computationally intensive portion of a backside surface of the semiconductor chip, wherein the heat conducting layer is compatible with semiconductor processing techniques, the heat conducting layer having a higher thermal conductivity than the semiconductor layer;

conducting heat generated by the number of electrical devices into the heat conducting layer;

transmitting the heat generated by the number of electrical devices through the heat conducting layer from a first region having a first temperature to a second region having a second temperature that is lower than the first region; and

transmitting heat through a substantially continuous interface between the heat conducting layer and an external heat sink.

2. (Original) The method of claim 1, wherein providing a number of electrical devices includes providing a number of transistors.

3. (Original) The method of claim 1, wherein coupling a heat conducting layer to the semiconductor layer comprises coupling a carbon containing layer to the semiconductor layer.

4. (Original) The method of claim 3 wherein coupling a carbon containing layer to the semiconductor layer comprises coupling a diamond containing layer to the semiconductor layer.

5. (Cancelled)

6. (Currently Amended) A method of cooling a semiconductor chip formed from a semiconducting material, comprising:

integrally coupling a substantially planar heat conducting layer to only a computationally intensive portion of a back side surface of a flip-chip configuration semiconductor chip, wherein the heat conducting layer is compatible with semiconductor processing techniques, the heat conducting layer having a higher thermal conductivity than the semiconducting material;

conducting heat from the semiconductor chip into the heat conducting layer;

transmitting the heat through the heat conducting layer from a first region having a first temperature to a second region having a second temperature that is lower than the first temperature; and

transmitting heat through a substantially continuous interface between the heat conducting layer and an external heat sink.

7. (Original) The method of claim 6, wherein coupling a substantially planar heat conducting layer to the semiconductor chip includes coupling a carbon containing layer to the semiconductor chip.

8. (Original) The method of claim 7, wherein coupling a carbon containing layer to the semiconductor chip includes coupling a diamond containing layer to the semiconductor chip.

9. (Cancelled)

10. (Currently Amended) A method of cooling a semiconductor chip, comprising:

integrally forming a diamond containing layer on only a computationally intensive portion of a backside of a flip-chip configuration semiconductor chip, the chip including a number of electrical devices;

conducting heat generated by at least a portion of the number of electrical devices in a first area into the diamond containing layer;

spreading the heat generated by the electrical devices in the first area through the diamond containing layer to a larger second area wherein heat per unit area is reduced; and

transmitting heat through a substantially continuous interface between the diamond containing layer and an external heat sink.

11. (Original) The method of claim 10, wherein integrally forming a diamond containing layer adjacent to a number of electrical devices includes integrally forming a diamond containing layer adjacent to a number of transistors.

12. - 13. (Cancelled)

14. (Previously Presented) The method of claim 10, wherein integrally forming a diamond containing layer adjacent to a number of electrical devices includes chemical vapor depositing a diamond containing layer on a back side of the semiconductor chip.

15. (Cancelled)

16. (Currently Amended) A method of manufacturing a semiconductor chip, comprising:

fabricating a semiconductor layer in a flip-chip configuration semiconductor chip;

forming a number of electrical devices on the semiconductor layer;

electrically connecting the number of electrical devices;

integrally forming a substantially planar heat conducting layer on only a computationally intensive portion of a backside surface of the flip-chip configuration semiconductor chip, wherein the heat conducting layer is compatible with semiconductor processing techniques, the heat conducting layer having a higher thermal conductivity than the semiconductor layer; and

coupling an external heat sink to the heat conducting layer to form a substantially continuous interface.

17. (Original) The method of claim 16, wherein fabricating a semiconductor layer includes fabricating a silicon substrate.

18. (Original) The method of claim 16, wherein forming a substantially planar heat conducting layer includes forming a carbon containing layer.

19. (Original) The method of claim 18, wherein forming a carbon containing layer includes forming a diamond containing layer.

20. (Original) The method of claim 19, wherein forming a diamond containing layer includes chemical vapor deposition (CVD) depositing a diamond layer.

21. (Currently Amended) A method of manufacturing a semiconductor chip, comprising:

forming a number of transistors on a semiconductor layer in a flip-chip configuration semiconductor chip;

electrically connecting the number of transistors; and

integrally forming a substantially planar diamond containing layer on only a computationally intensive portion of a backside surface of the flip-chip configuration semiconductor chip, and adjacent to the number of transistors; and

coupling an external heat sink to the diamond containing layer to form a substantially continuous interface.

22. (Original) The method of claim 21, wherein forming a number of transistors on a semiconductor layer includes forming a number of transistors on a silicon substrate.

23. (Cancelled)

24. (Previously Presented) The method of claim 21, wherein integrally forming a substantially planar diamond containing layer includes chemical vapor depositing a substantially planar diamond containing layer.

25. (Cancelled)

26. (Previously Presented) A method of forming an electronic system, comprising:

forming a flip-chip processor chip, including:

forming a number of transistors on a semiconductor layer;

electrically connecting the number of transistors;

integrally forming a substantially planar diamond containing layer on only a computationally intensive portion of a backside surface of the flip-chip processor chip;

coupling an external heat sink to the diamond containing layer to form a substantially continuous interface; and

coupling the flip-chip processor chip to a random access memory.

27. (Original) The method of claim 26, wherein forming a substantially planar diamond containing layer includes chemical vapor deposition (CVD) depositing a diamond layer.